REMARKS

Claims 1-16 are pending in this application. Claims 14-16 are subject to restriction and have been withdrawn by the Examiner. Claims 1, 11 and 13 are amended, claims 14-16 are cancelled and new claims 17-20 are added herein.

Claims 1, 11, 13 and 17 are independent.

The Examiner notes that certain art referenced in the background of the invention has not been cited in an Information Disclosure Statement. Accordingly, an Information Disclosure Statement is submitted herewith, which lists the art referenced in the background statement.

Claims 1-13 stand objected to on informality grounds.

Claims 1, 11 and 13 are amended to address the Examiner's noted concerns. The objection to claims 6 and 12 is respectfully traversed.

With regard to claim 6, it is respectfully submitted that the specific connectivity type is intentionally left unstated. It is further respectfully submitted that the claim, as originally filed, particularly points out and distinctly claims the subject matter which applicants regard as their invention, as will be understood by those skilled in the art. Accordingly, it is respectfully submitted that modification of claim 6 to state --substantially i-type-- is unnecessary.

With regard to claim 12, it is respectfully submitted that the claim properly recites that the conductive substrate, as recited in claim 11, is stainless steel, <u>and</u> that the substrate having a conductive layer on its surface, as recited in claim 11, is glass. That is, claim 11 recites alternative substrates and claim 12 further limits each of these

substrates to a particular material. Accordingly, claim 12 does not recite that the substrate is simultaneously steel and glass.

Claims 1, 3-5 and 7 stand rejected under 35 USC §102(a) as anticipated by Guliants et al. (Photovoltaic Specialist Conference, 15-22 September 2000, IEEE, pages 154-157). Claim 2 stands rejected under 35 USC §103(a) as obvious over Guliants et al. Claims 6 and 8-13 stand rejected under 35 USC §103(a) as obvious over Guilants et al. in view of Okamoto et al. (U.S. Patent No. 6,337,224). The rejections are respectfully traversed.

Each of claims 1, 8 and 11 require a first polycrystalline silicon layer which has been formed by introducing a metal catalyst element either into, or so as to come into contact with, a surface portion of an amorphous silicon layer which is in turn formed on the surface of a conductive substrate or a conductive layer on a substrate.

Guliants et al. discloses the formation of a solar cell generating layer by Metal Induced Growth (MIG). As is well understood in the art, MIG is a technique for obtaining Si film by forming a Ni film as a <u>prelayer</u> over a substrate and heating the substrate to approximately 525° C or more. See for example, the first full paragraph under "EXPERIMENT" on page 154 of Guliants.

Using the MIG technique, the substrate temperature must be high enough for the Ni film to act as a catalyst in order to obtain polycrystalline Si. Guliants et al. discloses that a 0.5 μm thick p-layer is formed after forming an n-layer (see for example, page 156, right column, lines 27-30). As described, "the surface morphology of the p-type film mimics the surface features of the metal-induced grown n-polysilicon" (see page

157, left column, lines 9-12). Thus, the p-type film, according to Guliants, is formed by the MIG technique. Thus, Guliants et al. discloses a solar cell in which at least one of the layers forming a p-n junction is crystallized using a prelayer of Ni film. Okamoto does not cure the defects in Guliants.

As noted above, independent claims 1, 11 and 13 each recite that the amorphous silicon layer, not a metal catalyst element or layer, is formed on the surface of the conductive substrate or conductive layer. Hence, each of these claims patentably distinguishes over the applied Guliants reference which requires that an Ni layer be formed on the substrate. Here again, Okamoto does not cure this defect.

However, to expedite allowance, each of the independent claims 1, 11 and 13 have been further amended to explicitly recite that the second, third, and/or fourth polycrystalline silicon layers are formed without catalytic effect. That is, the p-n junction or p-n junction forming layer (the generating layer) does not include Ni at all, since the metal catalyst element is not used for forming the generating layer or layers.

As now recited in independent claims 1, 11 and 13, the first polycrystalline layer, formed by introducing the metal catalyst element, serves as an early stage seed crystal layer which is subsequently used to form the generating layer or layers. These generating layers are formed by plasma CVD, without the Ni included in the seed crystal acting as a catalyst.

For example, as described on page 14, lines 20-24, of the subject application, the p-conductivity-type polycrystalline silicon was formed with a substrate temperature of approximately 200° C. As noted above, temperatures of approximately 525° C or

more are needed in order for Ni to act as a catalytic element. By avoiding the use of a metal catalyst element in the upper layers, metal contamination can be avoided. This in turn results in enhanced characteristics of the generating layer or layers and p-n junction or junctions.

New claims 17-20 recite the invention in a somewhat different manner.

Claim 17 requires a first polycrystalline silicon layer which is formed of an amorphous silicon layer disposed on the surface of the conductive substrate or conductive layer, and of a metal catalyst element which is introduced into or into contact with a surface portion of the amorphous silicon layer, with the amorphous silicon layer crystallized by heat treatment. As discussed above, it is respectfully submitted that the applied prior art, whether taken individually or in any combination lacks any teaching or suggestion of forming the amorphous silicon layer on the substrate or substrate conductive layer, and introducing a metal catalyst element into, or into contact with a surface portion of, the amorphous silicon layer as required by claim 17.

Claim 17 also requires a second polycrystalline silicon layer, which has the same conductivity type as the first polycrystalline silicon layer, and which is formed using the first polycrystalline silicon layer as a seed crystal. As has been previously discussed, it is respectfully submitted that the applied prior art fails to teach the use of a first polycrystalline silicon layer, as recited in claim 17, as a seed crystal in the formation of a second polycrystalline silicon layer.

Claims 18-20 also recite features which patentably distinguish over the applied prior art. For example, claim 18 requires that the second polycrystalline silicon layer is

formed by plasma CVD. As previously discussed, such a layer is not disclosed within the applied prior art.

Claim 19 requires that the second polycrystalline silicon layer be formed at a temperature of approximately 300° C or less. Here again, the applied art teaches the use of the MIG technique which requires substantially higher temperatures to form such a layer.

Claim 20 requires that the second polycrystalline silicon layer be formed without the metal catalyst element acting as a catalyst in its formation. As has been previously discussed, the applied prior art lacks any teaching or suggestion of such a limitation.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed local telephone number, in order to expedite resolution of any remaining issues and further to expedite passage of the application to issue, if any further comments, questions or suggestions arise in connection with the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 01-2135 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPENDIX TO RESPONSE TO OFFICIAL ACTION DATED August 14, 2002
AMENDMENTS TO CLAIMS
(DELETIONS IN BRACKETS AND ADDITIONS UNDERLINED)

IN THE CLAIMS

Please amend the claims as follows:

1. (Amended) A crystalline silicon thin film semiconductor device comprising:

a conductive substrate or a substrate having on its surface a conductive layer;

a crystallographically oriented first polycrystalline silicon layer, which has been formed by introducing a metal catalyst element (i) into, or (ii) so as to come into contact with a surface portion of, an amorphous silicon layer, the amorphous silicon layer being formed on the surface of the conductive substrate or the conductive layer, [or so as to come into contact with the surface portion of the amorphous silicon layer,] and heat treating the amorphous silicon layer to crystallize the amorphous silicon layer; and

a second polycrystalline silicon layer which has been formed without catalytic effect, using the first polycrystalline silicon layer as a seed crystal, so as to have the same conductivity type as the first polycrystalline silicon layer.

11. (Amended) A crystalline silicon thin film photovoltaic device comprising:

a conductive substrate or an insulating substrate having on its surface a conductive layer;

a first polycrystalline silicon layer of a first conductivity type which has been formed by introducing a metal catalyst element (i) into, or (ii) so as to come into contact with a surface portion of, an amorphous silicon layer, the amorphous silicon layer being formed on the surface of the conductive substrate or the conductive layer, [or so as to come into contact with the surface portion of the amorphous silicon layer,] and heat treating the amorphous silicon layer to crystallize the amorphous silicon layer;

a second polycrystalline silicon layer which has been formed without catalytic effect, using the first polycrystalline silicon layer as a seed crystal, so as to have the same conductivity type as the first conductivity type;

a substantially i-type third polycrystalline silicon layer formed, without catalytic effect, [provided] on the second polycrystalline silicon layer;

a fourth polycrystalline silicon layer that is [provided] formed, without catalytic effect, on the third polycrystalline silicon layer and is of a second conductivity type which is different from the first conductivity type; and

an electrode part provided on the fourth polycrystalline silicon layer.

13. (Amended) A crystalline silicon thin film photovoltaic device comprising:

an insulating substrate having on its surface an electrode;

a first polycrystalline silicon layer of a first conductivity type which has been formed by introducing a metal catalyst element (i) into, or (ii) so as to come into contact with a surface portion of, an amorphous silicon layer, the amorphous silicon layer being formed on the electrode of the insulating substrate, [or so as to come into contact with

the surface portion of the amorphous silicon layer,] and heat treating the amorphous silicon layer to crystallize the amorphous silicon layer;

a second polycrystalline silicon layer which has been formed without catalytic effect, using the first polycrystalline silicon layer as a seed crystal, so as to have the same conductivity type as the first conductivity type;

a third polycrystalline silicon layer which is [provided] formed without catalytic effect on the second polycrystalline silicon layer and is of a second conductivity type which is different from the first conductivity type; and

an electrode part provided on the third polycrystalline silicon layer.